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JUL 05 2006

Docket No. SUN-DA-1261
Serial No. 10/747,599

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for fabricating a semiconductor device comprising:
forming a first gate electrode including a dielectric layer, a first conducting layer, and an a
first insulating layer on a substrate, the first gate electrode functioning as a flash memory;
forming first spacers on sidewalls of the first gate electrode;
forming a second gate electrode comprising a gate oxide layer and a second conducting layer
on the substrate, the second gate electrode functioning as a normal gate electrode;
forming a first source/drain region with a shallow junction adjacent to one of the first spacers
and a second source/drain region with a shallow junction adjacent to the second gate electrode by
performing a first ion implantation process using at least one of the first spacers as a mask;
forming second spacers on a sidewall of the first spacer and on sidewalls of the second gate
electrode; and
completing a source/drain region with an LDD region by forming a source/drain region with a
deep junction adjacent to the first gate electrode, the source/drain region with the deep junction being
formed by a second ion implantation process using the at least one of the second spacers as a mask.
2. (Currently Amended) A method as defined in claim 1, wherein forming the first spacers
comprises:
forming a first second insulating layer on the substrate and the first gate electrode; and
performing an etch back process on the first second insulating layer.
3. (Currently Amended) A method as defined in claim 1, wherein forming the second spacers
comprises:
forming a second-third insulating layer on the substrate, the first gate electrode, the first
spacers, and the second gate electrode; and
performing an etch back process on the second-third insulating layer.
4. (Canceled).